WHAT IS CLAIMED IS:

1. A field effect transistor having reduced reverse body effects and reduced parasitic junction capacitance comprising:

a bulk silicon substrate;

a first source/drain region having a first depletion region associated therewith formed in said bulk silicon substrate;

a second source/drain region having a second depletion region associated therewith formed in said bulk silicon substrate;

a channel region separating said first and second source/drain regions;

a merged depletion region defined in said bulk silicon substrate, and under said channel region and between said first and second source/drain regions by merging said first and second depletion regions; and

a gate member formed over said channel region.

2. The field effect transistor of claim 1 wherein said merged depletion region is a fully merged depletion region.

3. The field effect transistor of claim 1 wherein said merged depletion region has an ion implantation density of between about E^{12}/cm^2 to about $5E^{13}/cm^2$.

4. The field effect transistor of claim 1 further comprising a pair of shallow trench isolation (STI) regions for isolating said field effect transistor.

5. The field effect transistor of claim 1 wherein said regions comprise first and second source/drain regions formed by optimally grading said source/drain regions to fully merge said depletion regions.

6. A multiplicity of field effect transistors having reduced reverse body effects and reduced parasitic junction capacitance, each of said multiplicity of field effect transistors comprising:

a bulk silicon substrate

a first source/drain region having a first depletion region associated therewith formed in said bulk silicon substrate;

a second source/drain region having a second depletion region associated therewith formed in said bulk silicon substrate;

a channel region formed in said bulk silicon substrate separating said first and second source/drain regions;

a merged depletion region defined in said bulk silicon substrate under said channel region and between said first and second source/drain regions by merging said first and second depletion regions;

a gate member formed over said channel region; and

a multiplicity of shallow trench isolation (STI) regions separating said multiplicity of field effect transistors from each other.

7. The multiplicity of field effect transistors of claim 6 wherein said merged depletion region has an ion implantation density of between about E^{12}/cm^2 to about $5E^{13}/cm^2$.

8. A method of manufacturing field effect transistors having reduced reverse body effects and reduced parasitic capacitance on a bulk silicon substrate comprising the steps of:

providing a bulk silicon substrate;

forming a multiplicity of source/drain region pairs, each separated by a channel region in said bulk silicon and having a depletion region associated therewith;

merging said depletion regions of said source/drain pairs by selective ion implantation; and

depositing a control gate over said channel region.

9. The method of claim 8 wherein said first and second source/drain regions are graded source/drain regions and wherein said step of ion implantation comprises the step of ion implanting said graded first and second source/drain regions in an optimal pattern and with an optimal density to merge said depletion regions.

10. The method of claim 8 wherein said step of merging said depletion region comprises the step of implanting ions at a density of between about E^{12}/cm^2 and about $5E^{13}/cm^2$.

11. The method of claim 8 wherein said step of merging comprises the step of fully merging said depletion regions.